39. (New) The method of claim 1, wherein the cap layer and the first antireflective coating form a graded change in an index of refraction.

40. (New) The method of claim 39, wherein the graded index of refraction reduce boundary reflections between the cap layer and the first antireflective coating.

41. (New) The method of claim 1, wherein the cap layer has a dielectric constant that is closer than a dielectric constant of the first antireflective coating to a subsequent photoresist mask layer dielectric constant.

REMARKS

This Amendment is responsive to the Communication mailed September 12, 2001, which withdrew from consideration claims 21-37 submitted July 2, 2001. In accordance with the Communication, claims 1-20 remain pending. By this Amendment prosecution of claims 1-20 is continued, along with new claims 38-41 which depend from claim 1. This balance of this Response addresses the rejections of the April 3, 2001 Office Action.

The specification has now been amended to reference the prior application, and thereby comply with the requirements of 35 U.S.C. § 120.

Claims 1-20 were rejected under the judicially created doctrine of obviousness-type double patenting over the claims of U.S. Patent No. 6,117,345. A Terminal Disclaimer is enclosed which addresses the rejection.

In paragraph 4, claim 8 was rejected under 35 U.S.C. § 112, second paragraph. Claim 8 has been amended to resolve this rejection.

In paragraph 5, claim 2 was rejected under 35 U.S.C. § 112, second paragraph. Claim 2 has been amended to resolve this rejection.

In paragraph 6, claims 1-8 and 20 were rejected under 35 U.S.C. § 112, first paragraph. The action asserts that the application does not reasonably provide enablement for method wherein the deposition step fails to fill the gaps. Applicant disagrees, and therefore traverses this rejection. The specification, at page 12, line 26 through page 13, line 5, describes that:

> The HDPCVD of layer 38 is performed until the gap 36 is substantially filled with a material that is preferably high density

> oxide having essentially no voids therein. By essentially void free the inventors mean that when compared with a conventionally deposited oxide layer, the HDPCVD oxide layer will be substantially free of voids. **As shown in Fig. 4, the gap my be filled to the level of the top of protective layer 26.** Depending on the subsequent processing steps to be performed, the area above the deposited layer 38 may be filled with layer 40. The layer 40 may be selected from a variety of materials and formed using a variety of techniques. Preferably the layer 40 is an oxide layer, which may be deposited at a higher speed than is typical of present HDPCVD processes. . . .
>
> .

This description clearly demonstrates that the gaps need not be completely filled, as suggested in paragraph 6 of the Action. Applicant submits that the pending claims satisfy the requirements of 35 U.S.C. § 112, first paragraph.

In paragraph 7, claims 1, 2 and 5-8 were rejected under 35 U.S.C. § 112, first paragraph. The Action asserts that the specification is enabling for methods wherein high density plasma chemical vapor deposition is used to deposit the dielectric material within the gaps between the wiring lines, it does not reasonably provide enablement for methods utilizing other deposition techniques to deposit the dielectric material. Independent claim 1 has been amended to address this rejection. Specifically, independent claim 1 has been amended to recite depositing a dielectric material within the gaps between the wiring lines *using a plasma based process having both an etching component and a deposition component*. These are distinguishing characteristics of a process currently referred to as high density plasma chemical vapor deposition. Support for this amendment may be found throughout the specification, e.g., at page 6, lines 15-27.

In paragraph 8, claims 1-19 were rejected under 35 U.S.C. § 112, first paragraph. The Action asserts that it is unclear how the antireflective coating (claim 1) and cap layer (claim 9) are selectively etched because the claims do not recite a mask layer or a photoresist layer. Applicant submits that the pending claims satisfy the requirements of 35 U.S.C. § 112, first paragraph. Therefore, applicants traverse this rejection.

Independent claim 1 recites the step of *etching through portions of the first antireflective coating, a portion of the cap layer, and a portion of the*

wiring line layer to form wiring lines separated by gaps. Independent claim 9 recites the step of *etching trough a portion of the cap layer and portions of the wiring line layer to form wiring lines separated by gaps* . . . . In an exemplary embodiment described at page 10, lines 16-24, a layer of photoresist is used to form a mask layer. However, it will be appreciated by one of ordinary skill in the art that alternate manufacturing techniques may not require the use of a mask layer to selectively etch the underlying layers to form wiring lines. Therefore, the use of a mask layer is not essential to the claimed invention.

In view of all of the above, claims 1-20 are allowable and the application is in condition for allowance, which action is respectfully requested. Newly presented claims 38-41 add additional limitations to claims 1-20. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

A Petition for Extension of Time requesting a 5-month extension to March 12, 2002, is enclosed. Note that a Petition for 2-Months Extension of Time was filed November 26, 2001, in which the $400 2-month fee was paid. Accordingly, the extension fee now due is believed to be $1,560 = $1,960 (the 5 month fee) -$400 (previously paid.) The enclosed check for $1,632.00 includes the Petition Fee differential of $1,560, the $110 Terminal Disclaimer Fee and $72 for 4 new claims over 20 (4 x $18). Please charge any fee deficiency or credit any overpayment associated with this transmittal to Deposit Account No. 50-1123.

Respectfully submitted,

March 12, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Paragraph beginning at page 1, line 1 has been amended as follows:

This application is a continuation of U.S. Serial No. 08/958,460, now U.S. Patent No. 6,117,345.

IN THE CLAIMS:

Claims 21-37 have been cancelled.

Claims 1-9, 11-12 and 20 have been amended as follows:

1. (Amended) A method for forming conducting structures separated by gaps on a substrate comprising:

providing a substrate and a wiring line layer above the substrate;

forming a first antireflective coating above [on] the wiring line layer;

forming a [second antireflective coating on] cap layer above the first antireflective coating, wherein [and the second antireflective coating are formed from different materials] the cap layer and the first antireflective coating have different dielectric constants;

etching through [a portion] portions of the first antireflective coating, a portion of the [second antireflective coating] cap layer and a portion of the wiring line layer to form wiring lines separated by gaps; and

depositing a dielectric material within the gaps between the wiring lines using a plasma based process having both an etching component and a deposition component.

2. (Amended) The method of claim 1, wherein the first antireflective coating absorbs portions of radiation applied during a lithographic process and the cap layer creates destructive interference with portions of radiation applied during the lithographic process. [works primarily by absorption and the second antireflective coating works primarily by interference.]

3. (Amended) The method of claim 1, wherein the [dielectric material within the gaps is deposited using high density plasma chemical vapor position.] cap layer cap layer also functions as a mask during the etching process.

4. (Amended) The method of claim 1, wherein [a] an additional portion of the [second antireflective coating] cap layer is etched during the plasma based process. [high density plasma chemical vapor deposition.]

5. (Amended) The method of claim 1, further comprising [the formation of] forming a surface layer between the substrate and the wiring line layer. [the surface layer being a barrier between the substrate wiring line layer.]

6. (Amended) The method of claim 1, further comprising the step of removing the [second antireflective coating] cap layer before [after the deposition of] depositing a dielectric material within the gaps.

7. (Amended) The method of claim 1, wherein [part] portions of the [second antireflective coating] cap layer [is] are removed and [remaining] portions of the [second antireflective coating] cap layer act as a mask during the etching of the first antireflective coating and the wiring line layer.

8. (Amended) The method of claim 1, wherein after etching each wiring line has a portion of the [second antireflective coating] cap layer thereon, the portion of a [second antireflective coating] cap layer on each wiring line having a cross-sectional shape selected from the group consisting of a rectangle, a triangle, trapezoid, and a rectangle having its upper corners etched away.

9. (Amended) A method for forming conducting structures separated by gaps on substrate comprising:

providing a substrate and a wiring line layer above the substrate;

forming a cap layer above the wiring line layer;

etching through a portion of the cap layer and a portions of the wiring line layer to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material [using high density plasma chemical vapor deposition within the gaps between the wiring lines at a sputtering rate sufficient] to substantially fill the gaps between the wiring lines, said dielectric material including a layer formed by high density plasma chemical vapor deposition.

11. (Amended) The method of claim 9, wherein the cap layer [is] comprises an antireflective coating.

12. (Amended) The method of claim 9, wherein [the remaining] portions of the cap layer [is] are partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

20. (Amended) A method of forming conducting structures separated by gaps filled with dielectrict material, comprising the steps of:

providing a substrate containing silicon, the substrate having a surface;

forming a surface layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten [allow,] alloy, the surface layer disposed on the substrate surface.

forming a metal wiring layer on the surface layer, the metal wiring layer having an upper surface;

forming a protective layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten [allow] alloy, the protective layer disposed on the upper surface of the metal wiring layer, the protective layer having a top surface;

forming a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, a silicon–rich oxide, and an oxynitride, the cap layer disposed on the top surface of the protective layer;

forming a patterned photoresist layer above the cap layer, said patterned photoresist layer covering selected portions of the cap layer and exposing other portions of the cap layer;

etching the cap layer, the protective layer and the metal wiring layer to form the conductive structures separated by gaps; and

forming a layer of high density plasma chemical vapor deposition (HDPCVD) dielectric material within the gaps.